Comments

Comparison of Thermal-Shunt and Flip-Chip HBT Thermal Impedances: Comment on "Novel HBT with Reduced Thermal Impedance"

T. Jenkins, C. Bozada, R. Dettmer, J. Sewell, D. Via, J. Barrette, J. Ebel, G. DeSalvo, C. Havasy, L. Liou, T. Quach, J. Gillespie, C. Pettiford, C. Ito, K. Nakano, and R. Anholt

I. Introduction

As indicated in the above letter,[1] reducing thermal impedance is a key to increasing heterojunction bipolar transistor (HBT) power densities. Also, as indicated by the above letter and others [1]–[3], several competing technologies are evolving to reduce the thermal impedance of HBT's. This comment specifically addresses the question: Does the flip-chip technology proposed in the above letter offer significantly lower HBT thermal impedance than the thermal-shunt technology?

II. Results

Fig. 1 shows measured thermal impedances for a variety of HBT layouts employing the thermal shunt technology and the results from the above letter. The thermal-shunt thermal impedances were measured on a thick wafer using Dawson's method [4], [5]. Three different layouts were measured: 1) HBT's with 4-μm-diameter emitter-dots in two fingers where the active area was scaled by increasing the number of emitter-dots per finger, 2) HBT's with four 4-μm-diameter emitter-dots per finger where the active area was scaled by adding additional fingers, and 3) HBT's with 3×13-μm^2 emitter-bars where the active area was increased by adding bars. The pitch of the emitter dots was 6 μm (center-to-center) and the fingers were spaced 30 μm apart. The thermal shunt thickness for all devices was 10 μm, and the thermal shunt width exceeded the base finger width by 8 μm. Each data point depicted in Fig. 1 was obtained by averaging the measured thermal impedance of five instances of each HBT from one wafer. The resultant uncertainty was less than 5%.

Specific thermal impedance is very useful in device design and was used to compare the results from the devices with variations in layout. For this purpose, a specific thermal impedance was defined by normalizing the results to the total emitter area. Therefore, specific thermal impedance allows a comparison of the temperature rise for different HBT's dissipating the same power density. Analogously, field effect transistor (FET) designs use specific thermal impedances that are normalized to the gate width (with units of °C-mm/W) and increase logarithmically with the total gate width [5]. This unit is equivalent to a gate-area normalization because the gate length is usually fixed.

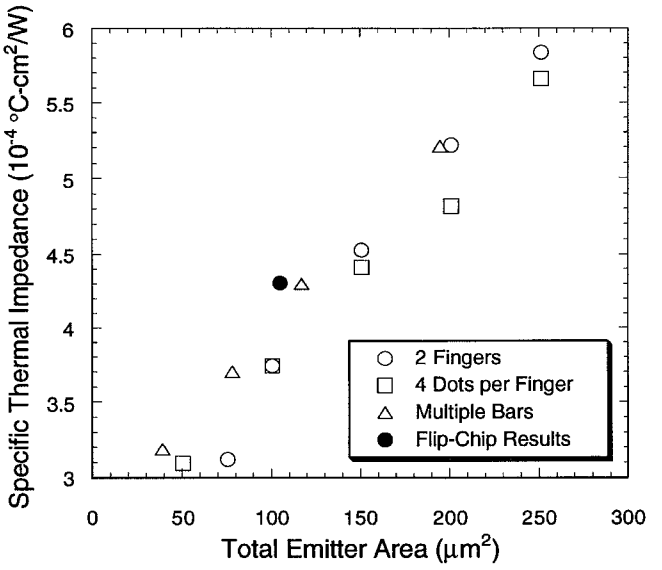

Fig. 1. Measured specific thermal impedances of thermal shunt and flip-chip HBT's.

As depicted in Fig. 1, all layouts (including the flip-chip results in the above letter) produced comparable specific thermal impedances. The differences are within the measurement uncertainties of 2–5%. Also, similar to results for FET's, the specific thermal impedance increased with device area. Also, at a constant power dissipation, the larger area designs yielded a lower temperature rise because the power density decreased directly with area while the specific thermal impedance increased very slowly with area. While the scalability of the thermal impedance using flip-chip technology was not demonstrated in the above letter, the thermal impedance of a single-finger flip-chip HBT was no better than a thermally shunted HBT.

Further experiments to optimize the thermal shunt technology have been conducted [6]. These experiments reduced the thermal impedance an additional 34% by increasing the thermal shunt thickness, increasing the finger spacing, and reducing the wafer thickness.

III. Conclusion

While any further reduction of the thermal impedance associated with flip-chip technology is yet to be determined, this comparison provides no compelling reason to adopt that technology.

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T. Jenkins, C. Bozada, R. Dettmer, J. Sewell, D. Via, J. Barrette, J. Ebel, G. DeSalvo, C. Havasy, L. Liou, T. Quach, J. Gillespie, C. Pettiford, C. Ito, and K. Nakano are with Solid State Electronics Directorate, Wright Laboratory, Wright-Patterson AFB, OH 45433 USA.

R. Anholt is with Gateway Modeling, Inc., Minneapolis, MN 55414 USA.

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